

NOTE: CAS0 - CAS7 ARE CONNECTED THRU 47Ω RESISTORS TO RCAS0 - RCAS7

- Y0D15 - CAS0
- Y1D14 - CAS1
- Y2D13 - CAS2
- Y3D12 - CAS3
- Y4D11 - CAS4
- Y5D10 - CAS5
- Y6D9 - CAS6
- Y7D7 - CAS7

- PRECAS/ SH.4
- LA18 SH.1
- LA17 SH.1
- LA16 SH.1
- PAREN SH.4

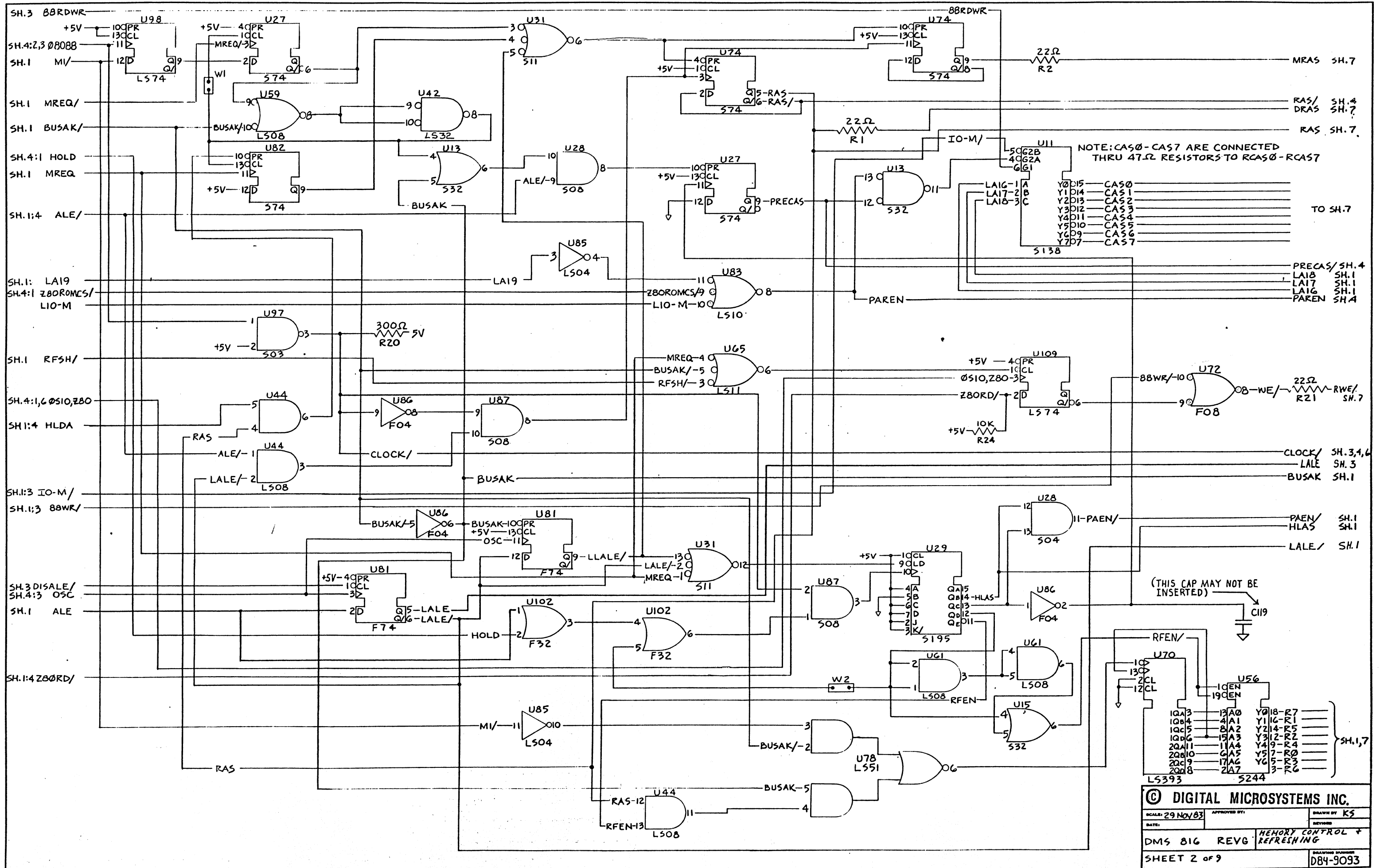
- 88WR/10
- WE/ RWE/ SH.7

- CLOCK/ SH.3,4,6
- LALE SH.3
- BUSAK SH.1

- PAEN/ SH.1
- HLAS SH.1
- LALE/ SH.1

(THIS CAP MAY NOT BE INSERTED)

- Y018-R7
- Y116-R1
- Y214-R5
- Y312-R2
- Y49-R4
- Y57-R0
- Y65-R3
- Y3-R6



NOTE: CAS0 - CAS7 ARE CONNECTED THRU 47Ω RESISTORS TO RCAS0 - RCAS7

(THIS CAP MAY NOT BE INSERTED)

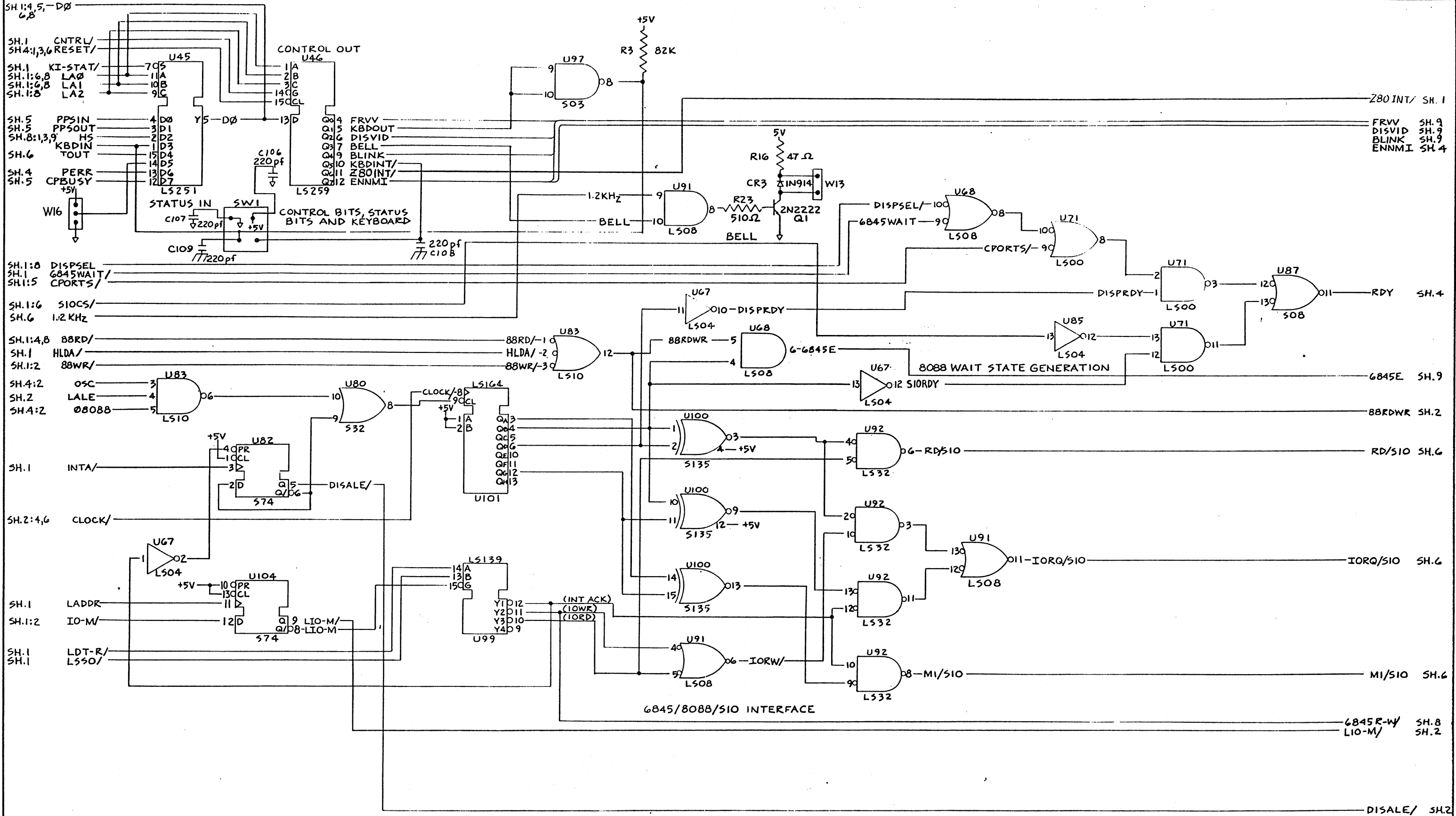
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SCALE: 29 NOV 83 APPROVED BY: DRAWN BY: KS

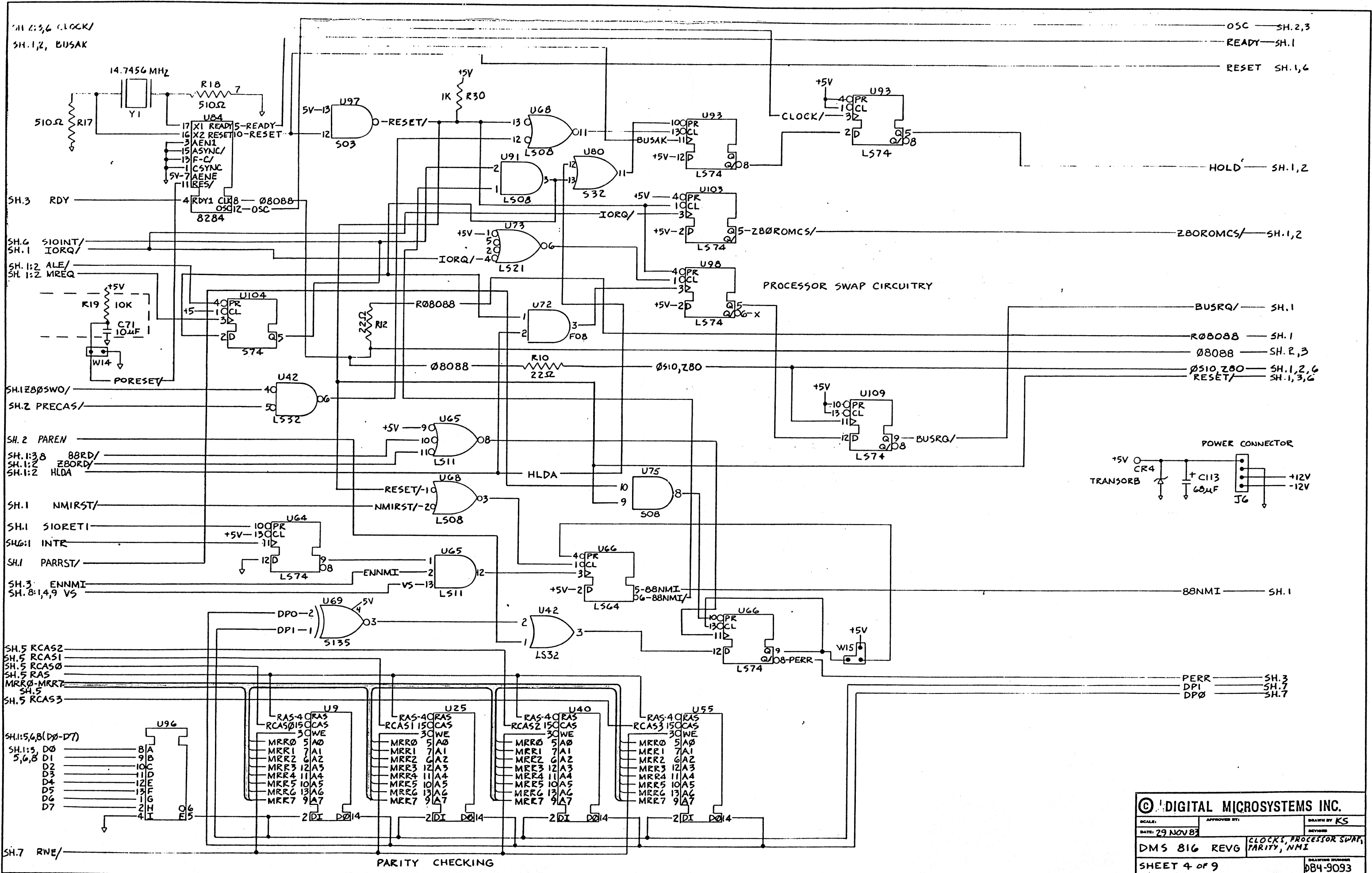
DATE: REVISION:

DMS 816 REV G MEMORY CONTROL + REFRESHING

SHEET 2 of 9 DRAWING NUMBER: DB4-9093



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SCALE:	APPROVED BY:
DATE: 30 NOV 83	REVISION:
DMS BIG REV G	8088 TO SIO-6845 INTERFACE WAIT STATE (8088) CONTROL + STATUS BITS, KEYBOARD, BELL
SHEET 3 OF 9	DRAWING NUMBER DB4-9093



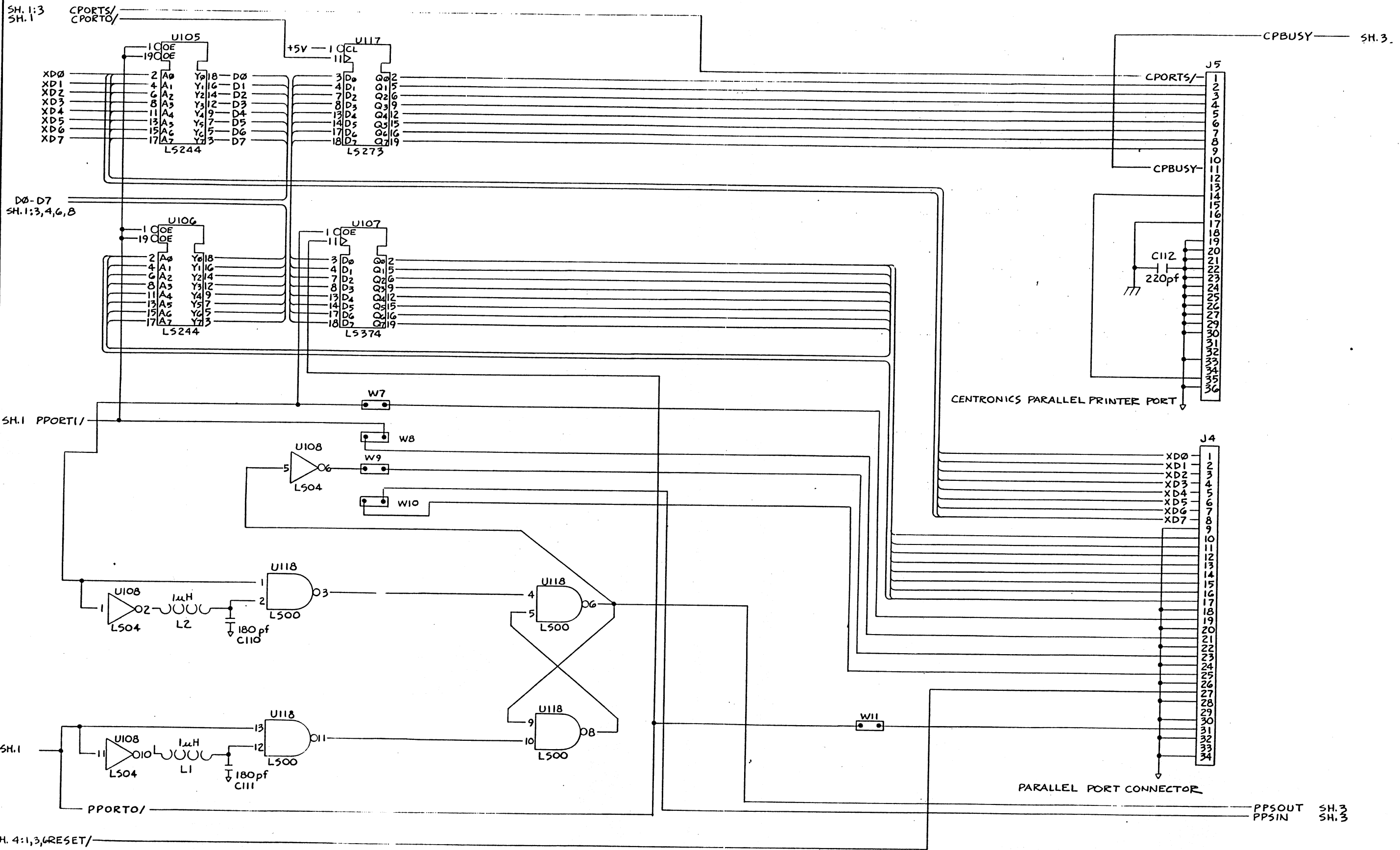
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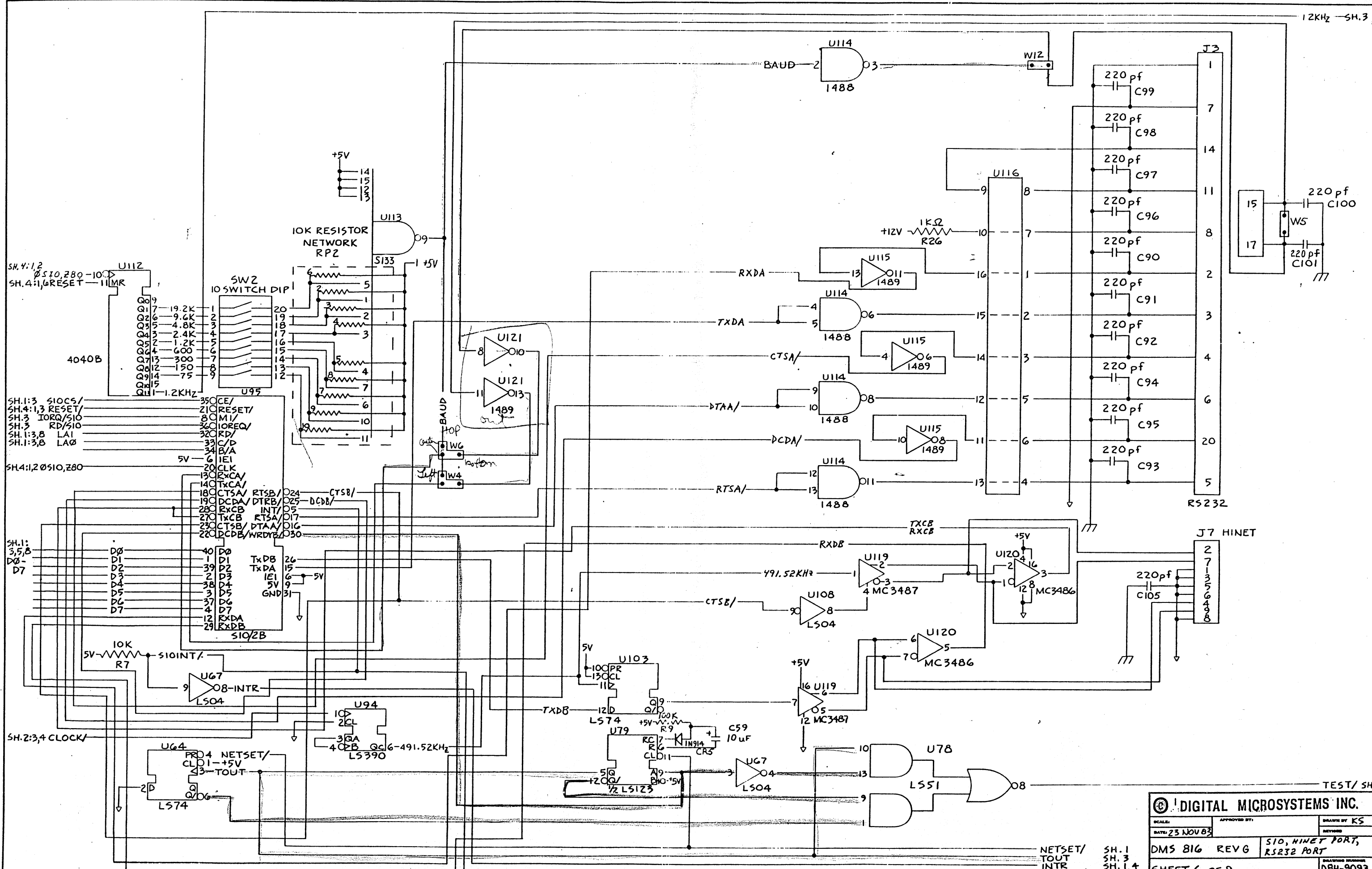
DATE: 29 NOV 87 REVISION: _____

DMS 816 REV G CLOCK, PROCESSOR SWAP, PARITY, NMI

SHEET 4 OF 9 DRAWING NUMBER: DB4-9093



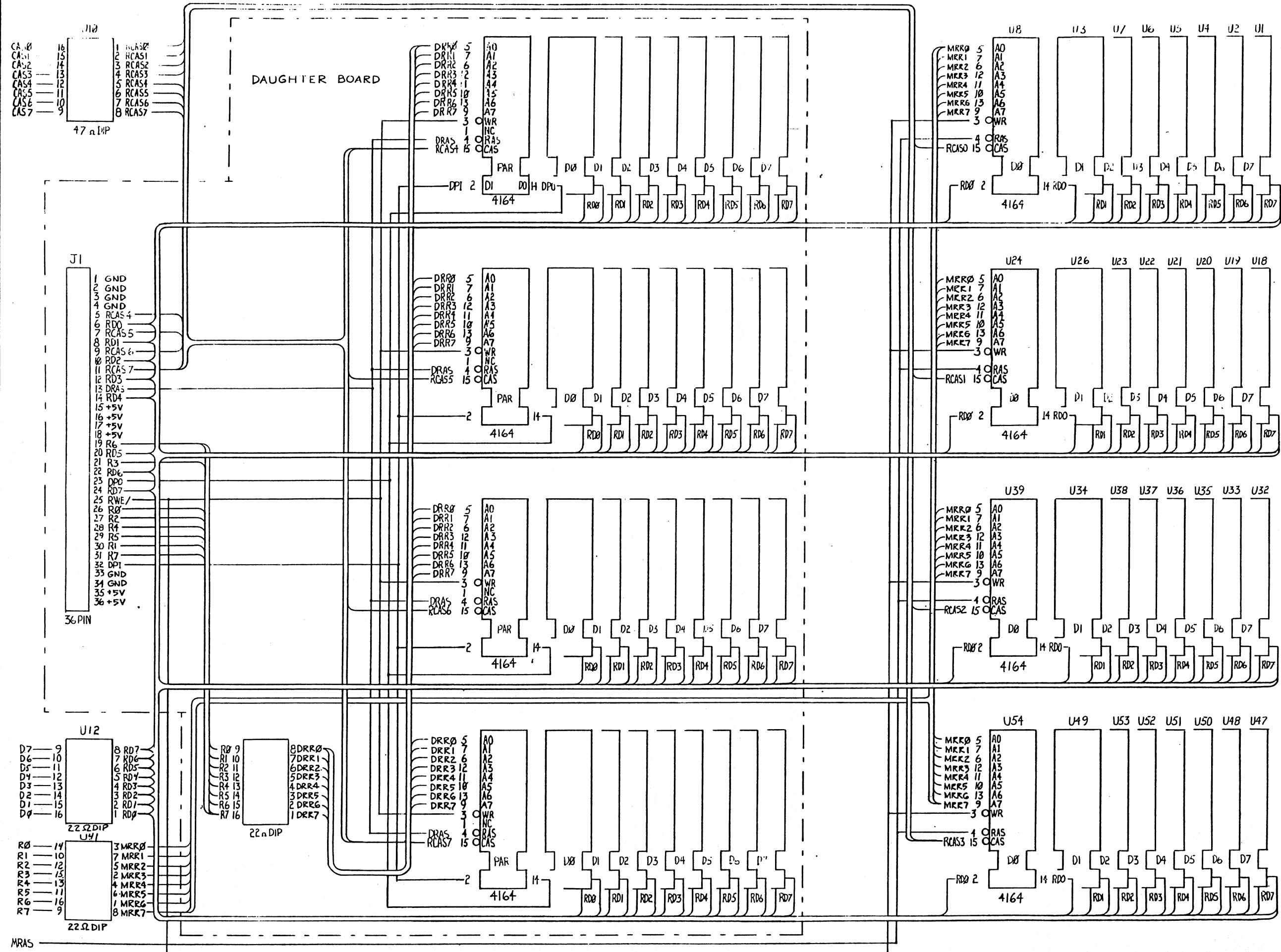
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SCALE:	APPROVED BY:	DRAWN BY KS
DATE: 23 NOV 83		REVIEW:
DMS 816 REV G	S10, HINET PORT, RS232 PORT	DRAWING NUMBER: DB4-9093
SHEET 6 OF 9		

NETSET/
TOUT
INTR
S10INT/
SH.1
SH.3
SH.1.4
SH.4

TEST/ SH.1



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DATE: 12-22-83 REVISION:

SH 7 OF 9 DMS 816

DAUGHTER & MAIN BD. MEM. DRAWING NUMBER: DB4-9033